Docket No. 246065US2S

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Kentaro NAKAJIMA et al.

SERIAL NO: 10/722,514 GAU:

FILED: November 28, 2003 EXAMINER:

FOR: MAGNETIC MEMORY DEVICE AND METHOD OF MANUFACTURING THE SAME

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

Applicant(s) wish to disclose the following information.

REFERENCES

☐ The applicant(s) wish to make of record the references listed on the attached form PTO-1449. Copies of the listed references are attached, where required, as are either statements of relevancy or any readily available English translations of pertinent portions of any non-English language references.

☐ A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

RELATED CASES

■ Attached is a list of applicant's pending application(s) which may be related to the present application. A copy of the claims and drawings of the pending application(s) is attached.

☐ A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

CERTIFICATION

☐ Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.

☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

DEPOSIT ACCOUNT

■ Please charge any additional fees for the papers being filed herewith and for which no check or credit card payment is enclosed herewith, or credit any overpayment to deposit account number 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Joseph A. Scafetta Jr.

Eckhard H. Kuesters
Registration No. 28,870
Joseph A. Scafetta, Jr.
Registration No. 26, 803

Customer Number
22850
Tel. (703) 413-3000
Fax. (703) 413-2220
(OSMMN 05/03)

LIST OF RELATED CASES

Docket Number	Serial or Patent Number	Filing or Issue Date	Inventor/ Applicant
240063US2	10/615,920	07/10/03	HOSOTANI et al.
246065US2S*	10/722,514	11/28/03	NAKAJIMA et al.

*Present Application; listed for information

EHK/akh

I:\EM\EMREL\245S246S\246065US LIST.DOC

What is claimed is:

1. A magnetic memory device comprising:

a semiconductor substrate;

a transistor formed above said semiconductor substrate;

a tunnel magneto-resistive element formed above an interlayer dielectric film covering said transistor of said semiconductor substrate;

a first wiring line buried in said interlayer dielectric film and connected to a source/drain diffusion layer of said transistor;

a second wiring line buried under said tunnel magneto-resistive element while overlying said first wiring line in said interlayer dielectric film, to provide a current magnetic field to said tunnel magneto-resistive element during writing; and

a third wiring line connected to an upper surface of said tunnel magneto-resistive element and provided to cross said second wiring line, to provide a current magnetic field to said tunnel magneto-resistive element during writing and also to cause a cell current to flow during reading,

wherein said second wiring line is formed and patterned so that its both edges are placed outside the pattern of said tunnel magneto-resistive element.

2. The device according to claim 1, wherein said first wiring line is formed by patterning so that its both edges are placed outside of the pattern of said tunnel magneto-resistive element.

3. The device according to claim 2, wherein a gate wiring line of said transistor is patterned to pass through a region immediately beneath said tunnel magneto-resistive element while having a width greater than that of said tunnel magneto-resistive element.

4. The device according to claim 2, wherein a gate wiring line of said transistor is patterned to extend outside of a region immediately beneath said tunnel magneto-resistive element.

5. The device according to claim 2, wherein the first and second wiring lines are formed by patterning to pass through a region immediately beneath said tunnel magneto-resistive element while having a width greater than that of said tunnel magneto-resistive element.

6. The device according to claim 3, wherein a gate wiring line of said transistor is patterned to pass through a region immediately beneath said tunnel magneto-resistive element while having a width greater than that of said tunnel magneto-resistive element.

7. The device according to claim 3, wherein a gate wiring line of said transistor is patterned to extend outside of a region immediately beneath said tunnel magneto-resistive element.

8. A magnetic memory device comprising:

a semiconductor substrate;

a transistor formed above said semiconductor substrate;

a tunnel magneto-resistive element formed above an interlayer dielectric film covering said transistor of said semiconductor substrate;

a first wiring line buried in said interlayer dielectric film and connected to a source/drain diffusion layer of said transistor;

a second wiring line buried under said tunnel magneto-resistive element while overlying said first wiring line in said interlayer dielectric film, to provide a current magnetic field to said tunnel magneto-resistive element during writing; and

a third wiring line connected to an upper surface of said tunnel magneto-resistive element and provided to cross said second wiring line, to provide a current magnetic field to said tunnel magneto-resistive element during writing and to cause a cell current to flow during reading, wherein

all of element regions including all wiring lines including the first and second wiring lines formed under said tunnel magneto-resistive element above said semiconductor substrate, a gate wiring line of said transistor, more than one wiring contact and the source/drain diffusion layer are formed by patterning so that edges thereof are placed outside of a region immediately underlying said tunnel magneto-resistive element.

ABSTRACT OF THE DISCLOSURE

A magnetic memory device capable of achieving high reliability and superior operation characteristics of tunneling magneto-resistive (TMR) elements is provided. This magnetic memory device includes a semiconductor substrate, a transistor which is formed above the semiconductor substrate, and a TMR element which is formed on or above an interlayer dielectric film that covers the transistor of the substrate. The device also includes a first wiring line which is buried in the interlayer dielectric film and connected to a source/drain diffusion layer of the transistor, a second wiring line which is buried under the TMR element while overlying the first wiring line within the interlayer dielectric film and which is used to apply a current-created magnetic field to the TMR element during writing, and a third wiring line connected to an upper surface of the TMR element and provided to cross the second wiring line. The third wiring line is for applying a current magnetic field to the TMR element during writing and also for causing a cell current to flow during reading. The second wiring line is formed by patterning techniques so that its both edges are placed outside of a pattern of the TMR element.

FIG. 1

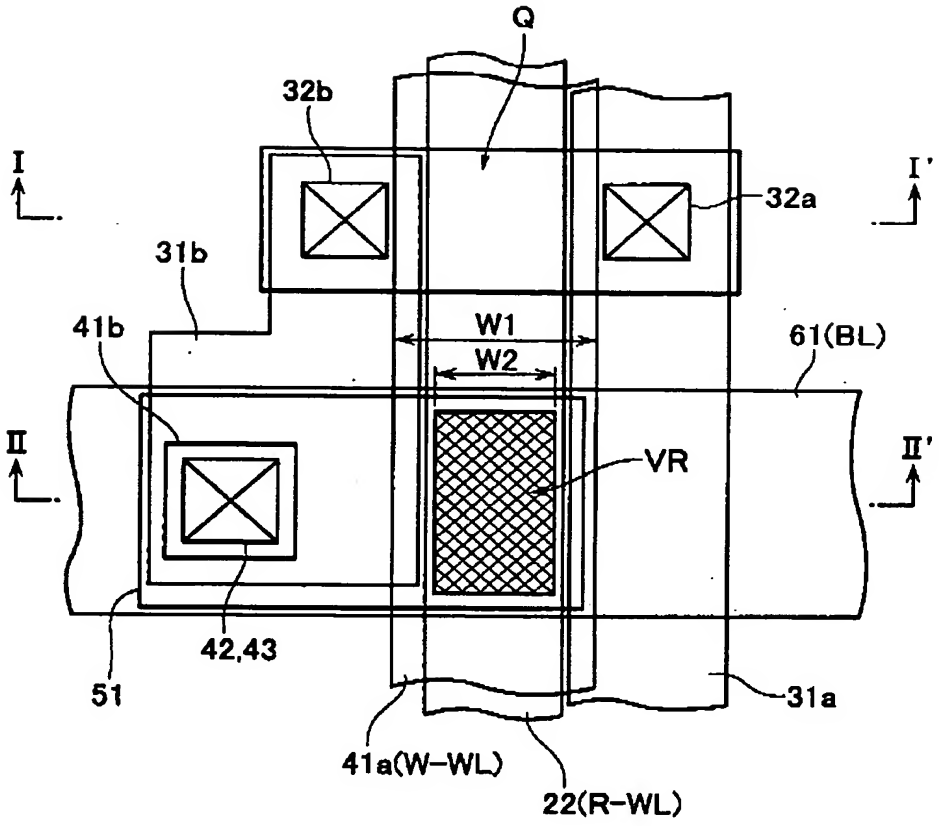

FIG. 2A

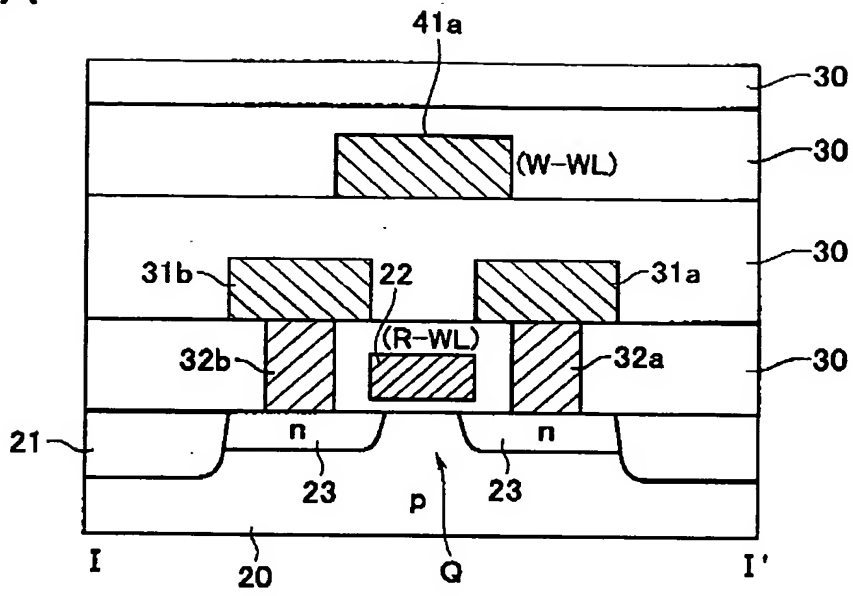
41a
30
(W-WL)
30
31b
22
31a
30
(R-WL)
32b
32a
30
21
n
n
23
23
p
I
20
Q
I'

FIG. 2B

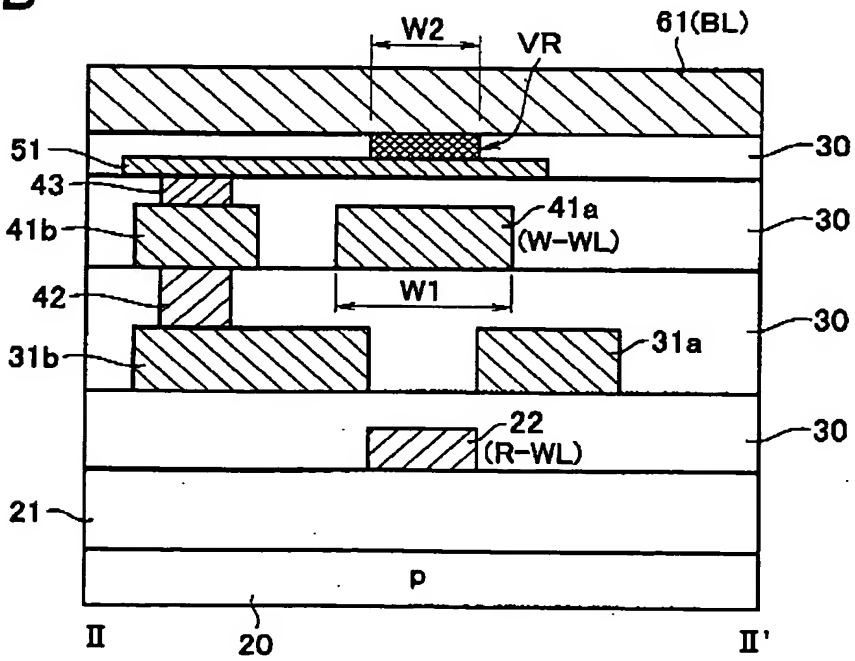
W2
VR
61(BL)
51
30
43
41b
41a
(W-WL)
30
W1
42
31b
31a
30
22
(R-WL)
30
21
p
II
20
II'

FIG. 3

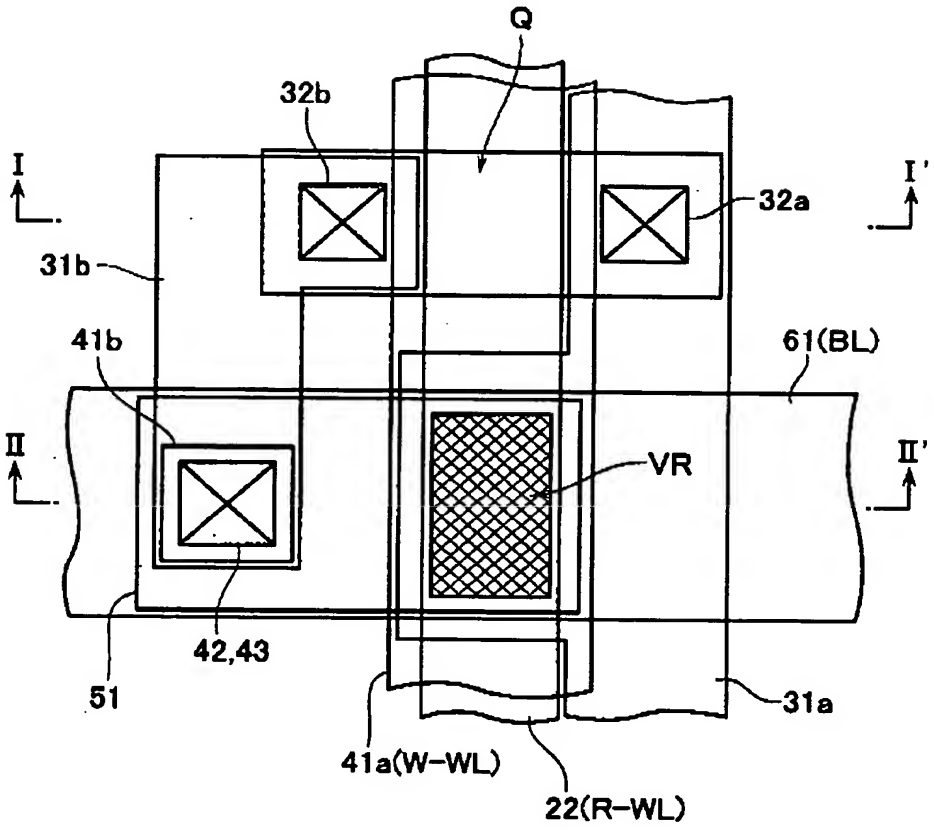

FIG. 4A

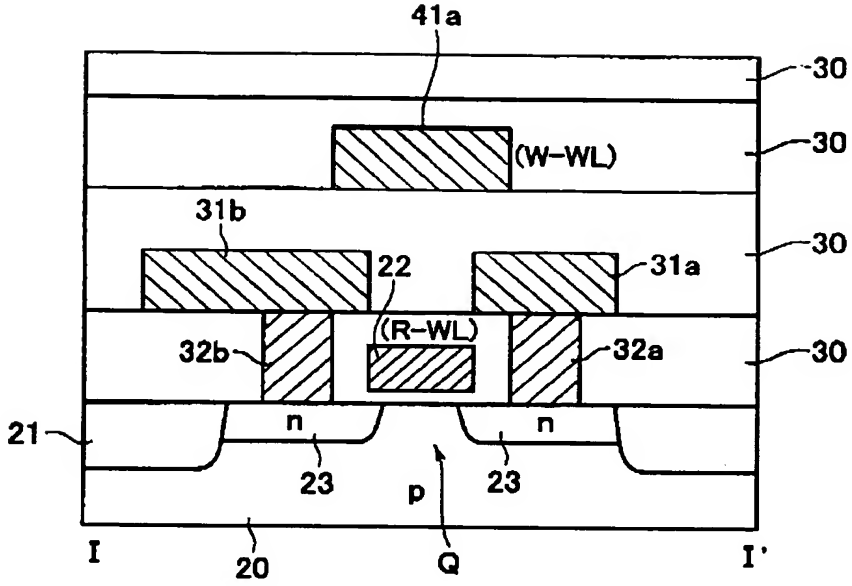
41a
30
(W-WL)
30
31b
22
31a
30
(R-WL)
32b
32a
30
21
n
n
23
23
p
I
20
Q
I'

FIG. 4B

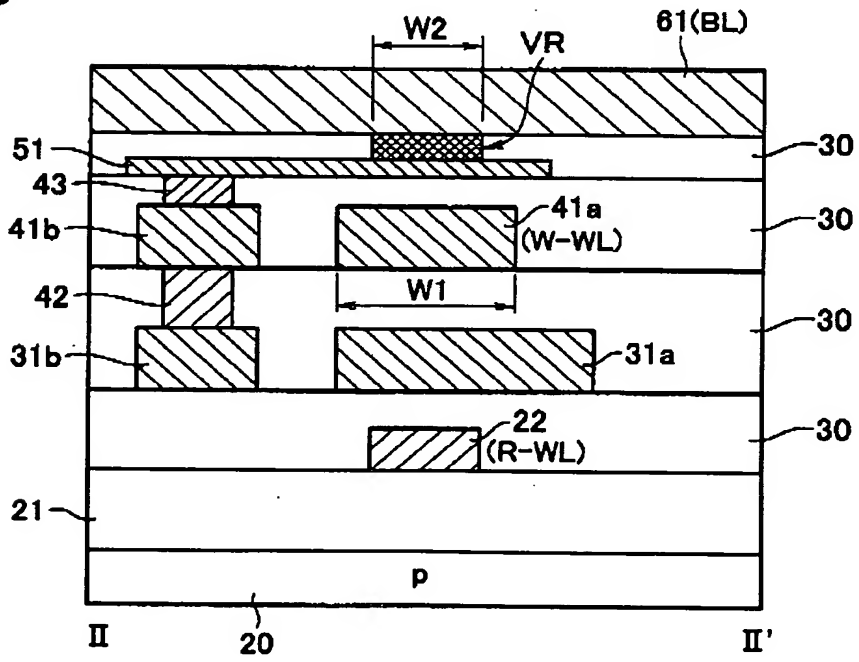
W2
VR
61(BL)
51
30
43
41a
41b
(W-WL)
30
W1
42
30
31b
31a
22
(R-WL)
30
21
p
II
20
II'

FIG. 5

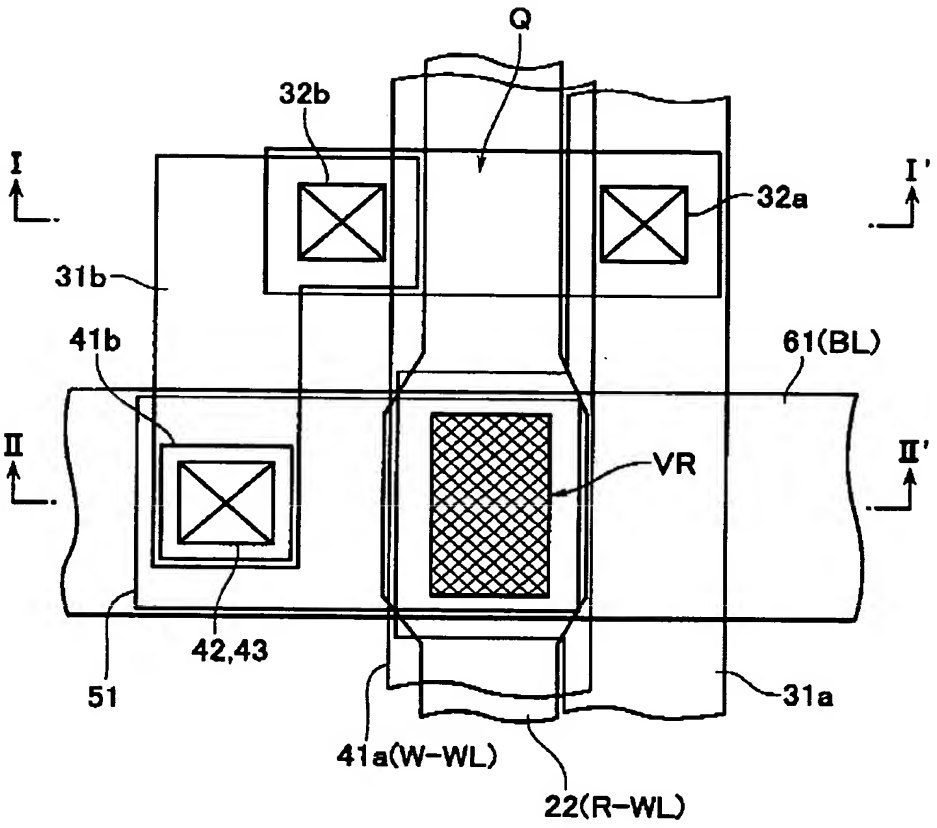

FIG. 6A

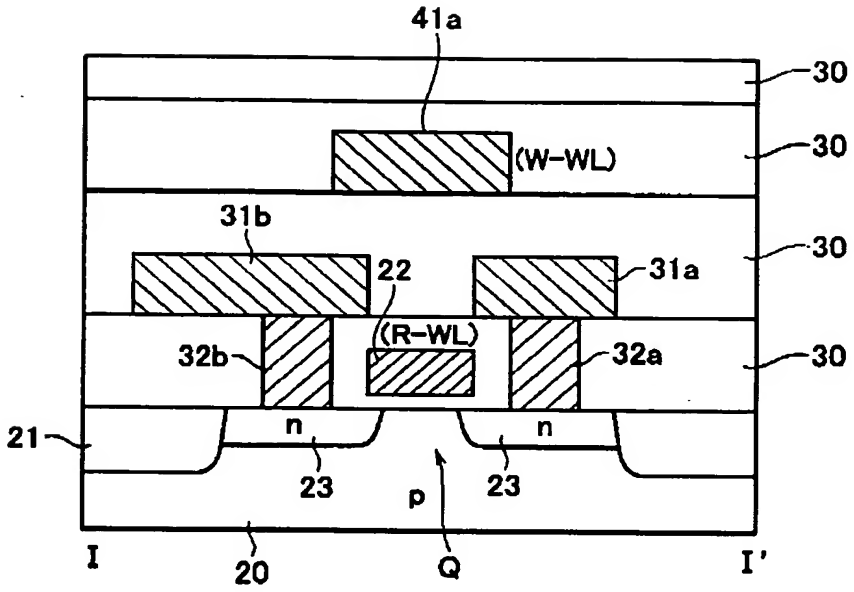
41a
30
(W-WL)
30
31b
22
31a
30
(R-WL)
32b
32a
30
21
n
n
23
p
23
I
20
Q
I'

FIG. 6B

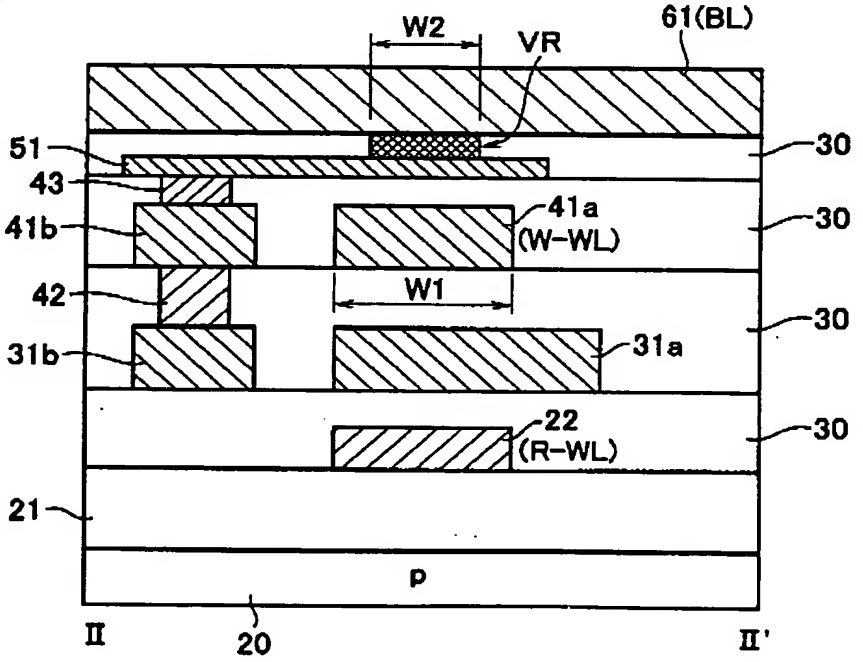
W2
VR
61(BL)
51
30
43
41b
41a
(W-WL)
30
W1
42
30
31b
31a
22
(R-WL)
30
21
p
II
20
II'

FIG. 7

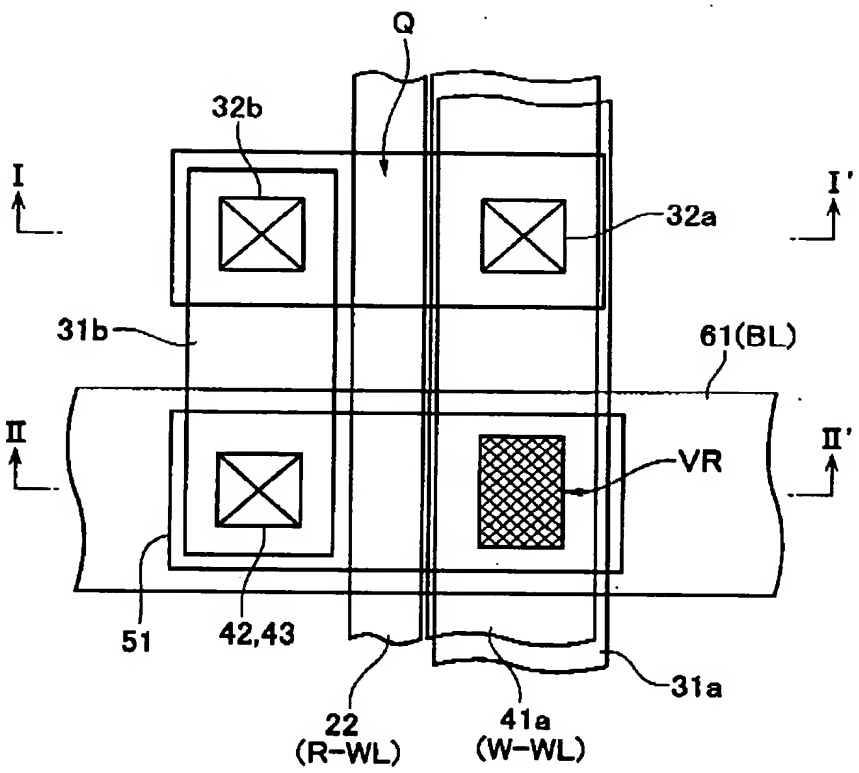

FIG. 8A

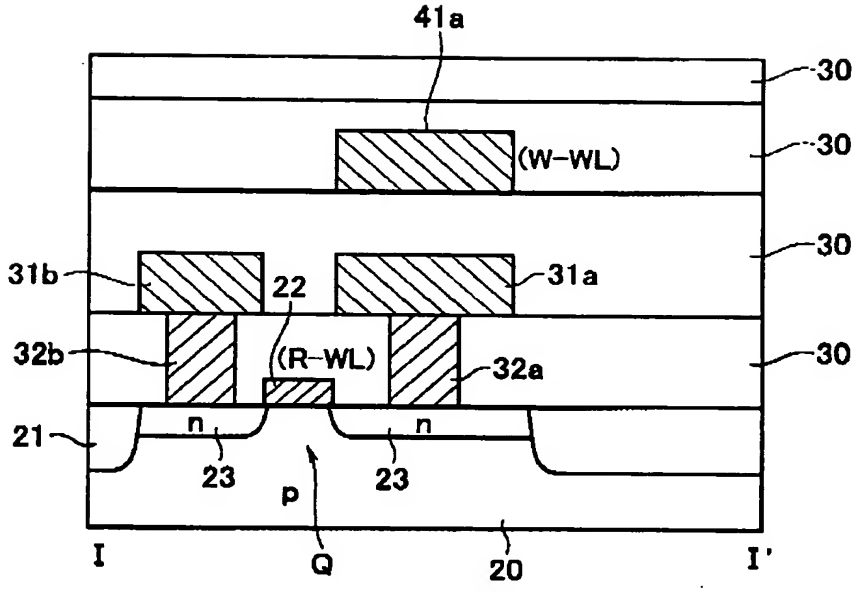
41a
30
(W-WL)
30
30
31b
22
31a
32b
(R-WL)
32a
30
21
n
n
23
23
p
I
Q
20
I'

FIG. 8B

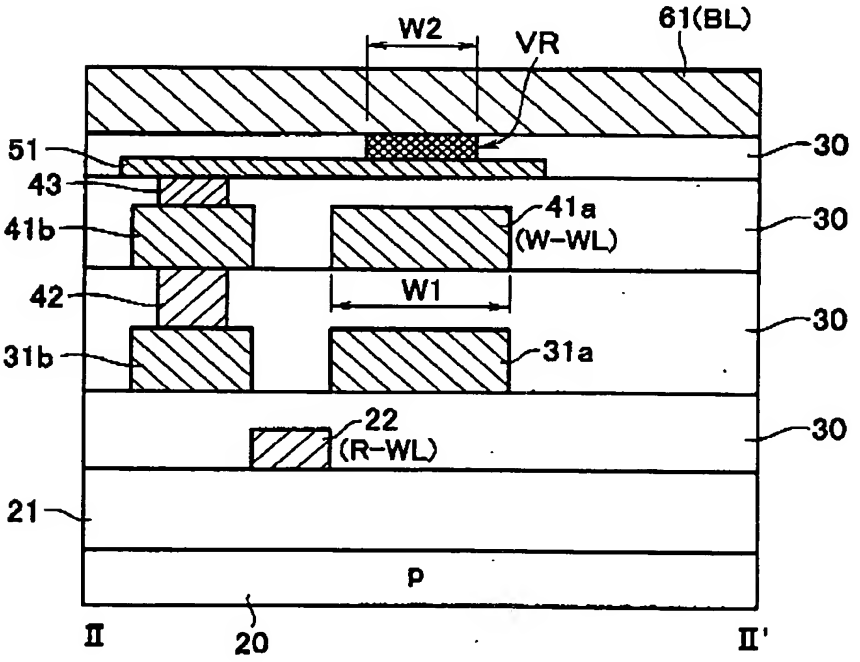
W2
VR
61(BL)
51
30
43
41a
41b
(W-WL)
30
W1
42
30
31b
31a
22
(R-WL)
30
21
p
II
20
II'

FIG. 9

(PRIOR ART)

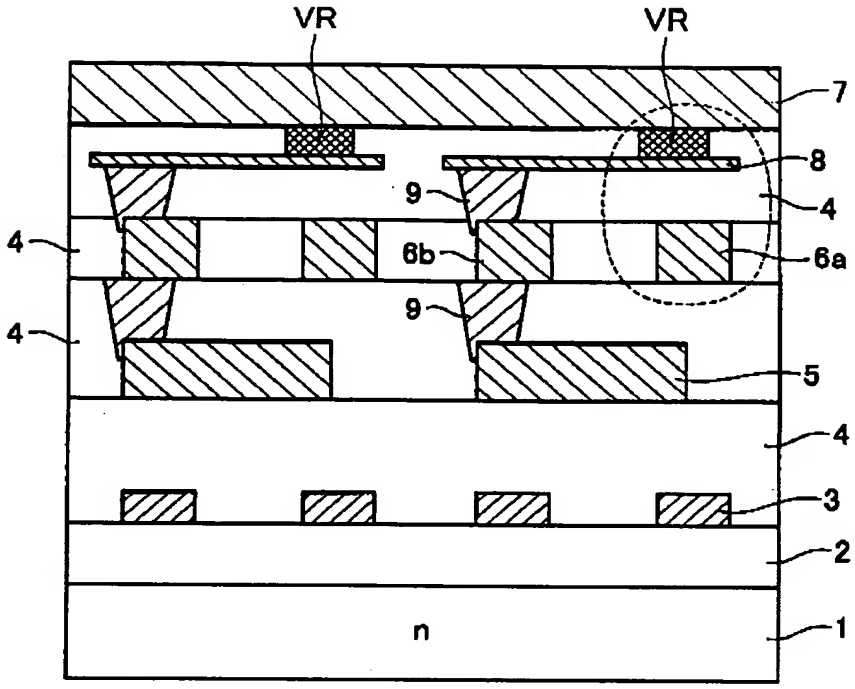

FIG. 10

(PRIOR ART)